**Amendments to the Specification:**

**Please rewrite the paragraph beginning on page 1, line 26 as follows:**

When a certain input signal is supplied from the input terminal 102 of the variable delay line 100, the output terminal 104 outputs an output signal having a predetermined absolute delay time shown in FIG. 16. If the coupling capacitance C of the variable-capacitance capacitor 110 shown in FIG. 17 is changed, then the absolute delay time changes as shown in FIG. 18. For example, if the coupling capacitance C is changed from C1 to C2 or C3 (C1 > C2 > C3), then the absolute delay time increases as shown by the different curves in Fig. 16. If the coupling capacitance C has a wider adjustable range, then the absolute delay time of the variable delay line 100 has a wider variable range (hereinafter referred to as "variable delay time").

**Please rewrite the paragraph beginning on page 2, line 17 as follows:**

If the coupling capacitance C is changed, then the capacitor 106 and the first resonant circuit 112 near the input terminal 102 shown in FIG. 15 and the capacitor 108 and the second resonant circuit 114 near the output terminal 104 are brought out of balance, thereby varying the values of the input and output impedances of the variable delay line 100. Thus, it is difficult to achieve impedance matching on the variable delay line 100. Therefore, the return loss shown in FIG. 18 increases. Furthermore, the frequency response shown in FIG. 17 are greatly attenuated, resulting in an increased insertion loss over the variable delay line 100 and an increased deviation of the absolute delay time shown in FIG. 16.

**Please rewrite the paragraph beginning on page 3, line 23 as follows:**

~~DISCLOSURE~~SUMMARY OF THE INVENTION:

It is an object of the present invention to provide a variable delay line having a hybrid coupler and variable-reactance devices which are connected respectively to two output terminals of the hybrid coupler for ~~thereby~~ suppressing variations in an input impedance and an output impedance of the variable delay line, reducing a deviation of

the absolute delay time, increasing the variable delay time of the variable delay line, and widening the passband of the variable delay line.

**Please add the following paragraph after the heading on page 10, line 7:**

The invention will now be described in detail based on several embodiments, with reference to the attached drawings. In the drawings, the same or the similar numerical references refer to the same or similar elements.

**Please rewrite the paragraph beginning on page 12, line 18 as follows:**

~~When~~With reference to Fig. 2, when the coupling capacitances C of the first and second variable-capacitance devices 26, 28 of the first and second reactance parts 18, 20 are changed by the same value, the reactances X of the first and second reactance parts 18, 20 are changed by the same value. Therefore, the third output signal can be changed by a desired value. Accordingly, the absolute delay time of the third output signal from the variable delay line 10 in Fig. 1 can be changed by a certain value, and the variable delay time can be set to a desired value. When the coupling capacitances C of the first and second variable-capacitance devices 26, 28 are changed by a certain value, the variable delay line 10 can have a desired absolute delay time and a desired variable delay time.

**Please rewrite the paragraph beginning on page 13, line 5 as follows:**

The first and second resonant circuits 30, 32 (see Fig. 2) have respective resonant frequencies. The central frequency of the passband of the variable delay line 10 is determined by these resonant frequencies. Therefore, the variable delay line 10 can have a desired passband by setting the resonant frequencies to a desired value.

**Please rewrite the paragraph beginning on page 17, line 12 as follows:**

Specifically, when the coupling capacitances Cv of the third and fourth varactor diodes 58, 60 change from Cv = C4 to Cv = C5 or Cv = C6 (C4 > C5 > C6), it is

possible to change the phase of the third output signal without affecting the absolute delay time of the variable delay line 10B, as shown in FIGS. 8 and 9. Consequently, the absolute delay time of the variable delay line 10B can be changed while keeping the phase of the third output signal at a certain value, so that the variable delay line 10B can have a desired absolute delay time and a desired variable delay time as shown in Fig. 8.

**Please rewrite the paragraph beginning on page 18, line 1 as follows:**

As shown in FIG. 10, the first and second voltage control terminals 50, 52 are connected respectively to the cathode terminals K1, K2 of the first and second varactor diodes 42, 44 through respective resistors 74, 76. As shown in FIGS. 11 through ~~15~~14, the variable delay line 10C has an integral ceramic board (integral structural body) 78 produced by stacking a plurality of ceramic layers S1, ~~through~~S2, S3, S4, S5, S6, S7, S8, S9, S10 and S11 as shown in Fig. 13 and sintering them into an integral body.

**Please rewrite the paragraph beginning on page 18, line 16 as follows:**

The ceramic board 78 has an upper surface 78e (see Fig. 12) covered substantially entirely with a metal case 80 (see Fig. 11) which serves as an upper lid for the ceramic board 78. The case 80 has four sides including respective legs 80a through 80d disposed centrally on lower portions thereof. When the ceramic board 78 and the case 80 are mounted on each other so that the legs 80a, ~~through~~80b, 80c and 80d are held in abutment against the upper surface 78e, the upper surface 78e is covered substantially entirely by the case 80, with gaps 81 (see Fig. 11) being defined between four corners of the four sides of the case 80 which are free of the legs 80a through 80d and four corners of the upper surface 78e.

**Please rewrite the paragraph beginning on page 19, line 1 as follows:**

Of first through fourth side surfaces 78a, ~~through~~78b, 78c and 78d as surfaces of the ceramic board 78, the first and fourth side surfaces 78a, 78d have surface ground electrodes 82a, 82d, respectively, disposed centrally therein and extending from the upper surface 78e to a lower surface 78f (see Fig. 11) of the ceramic board 78, as shown in FIGS. 11 and 12.